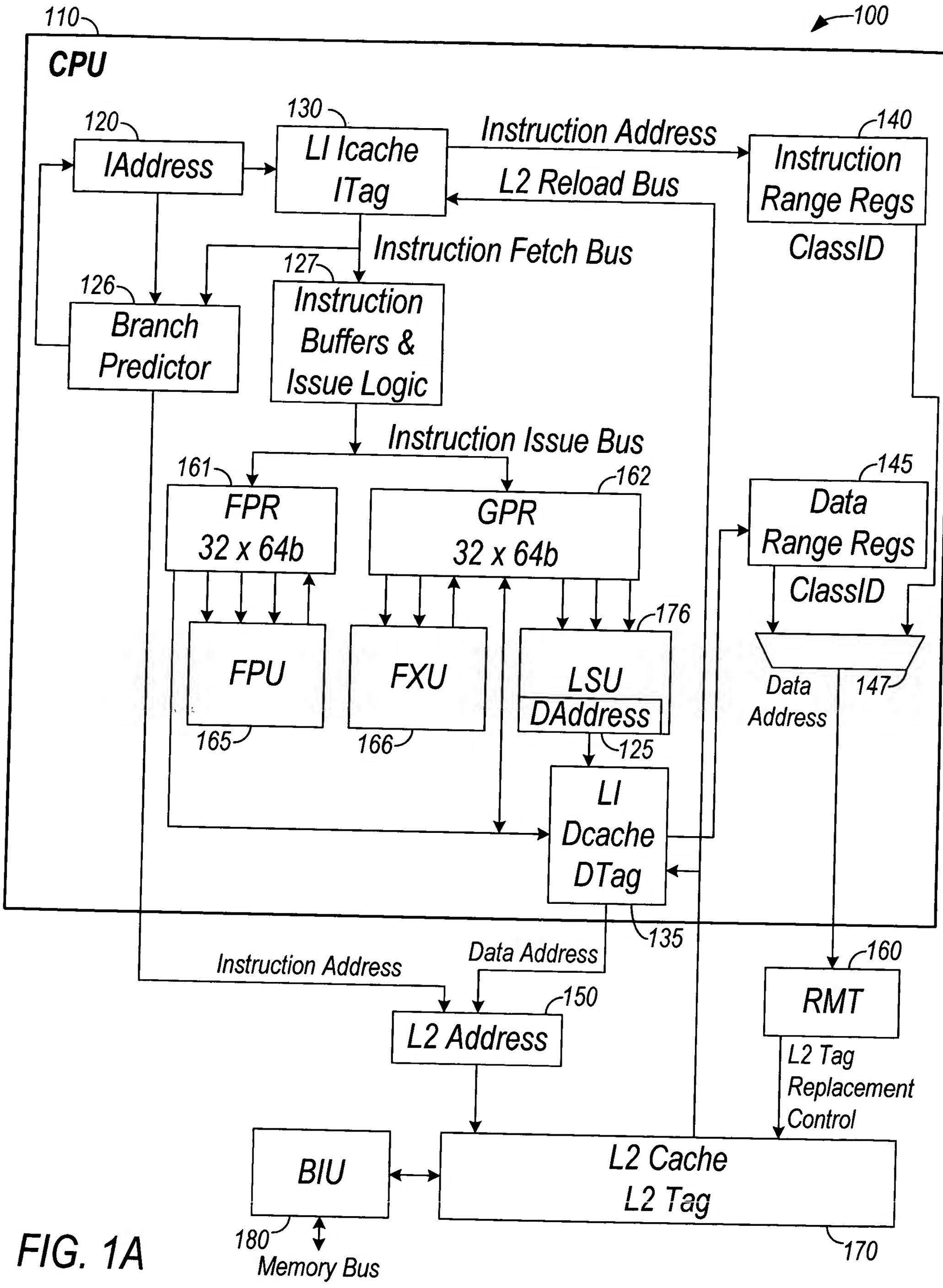
110
CPU
100
120
IAddress
130
LI Icache
ITag
Instruction Address
L2 Reload Bus
140
Instruction
Range Regs
ClassID
Instruction Fetch Bus
127
Instruction
Buffers &
Issue Logic
126
Branch
Predictor
Instruction Issue Bus
161
FPR
32 x 64b
162
GPR
32 x 64b
145
Data
Range Regs
ClassID
176
FPU
FXU
LSU
DAddress
165
166
125
LI
Dcache
DTag
Data
Address
147
135
Instruction Address
Data Address
160
RMT
150
L2 Address
L2 Tag
Replacement
Control
BIU
L2 Cache
L2 Tag
180
Memory Bus
170

FIG. 1A

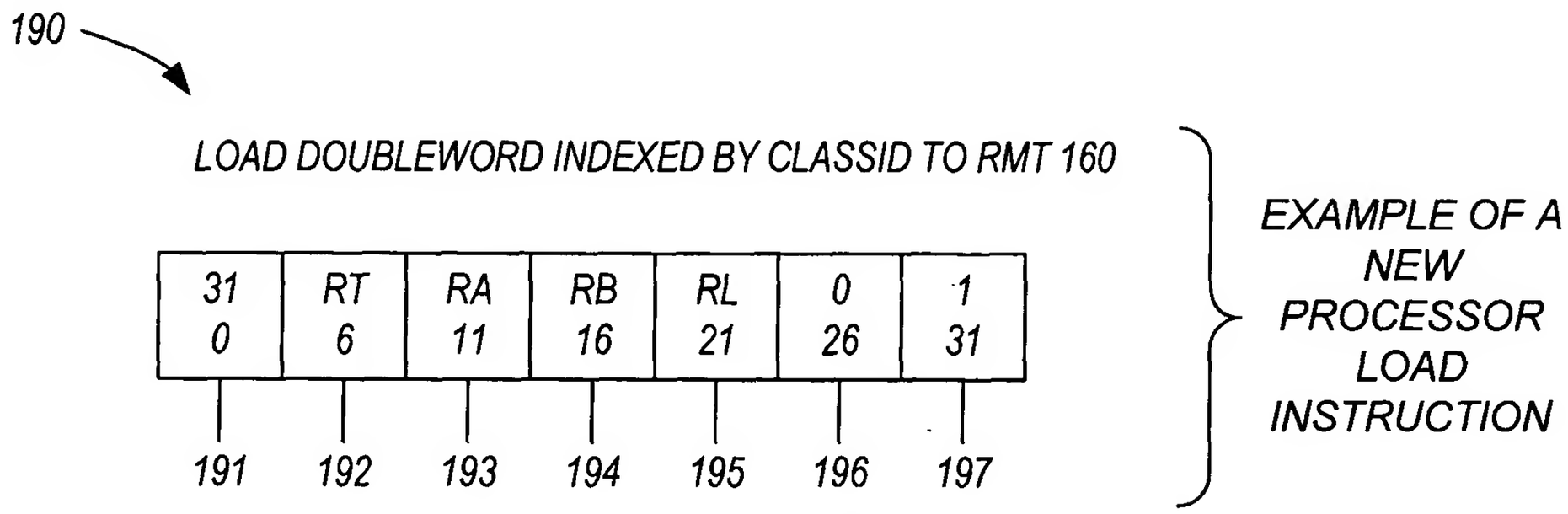
190
LOAD DOUBLEWORD INDEXED BY CLASSID TO RMT 160
31
0
RT
6
RA
11
RB
16
RL
21
0
26
1
31
191
192
193
194
195
196
197
EXAMPLE OF A NEW PROCESSOR LOAD INSTRUCTION

FIG. 1B

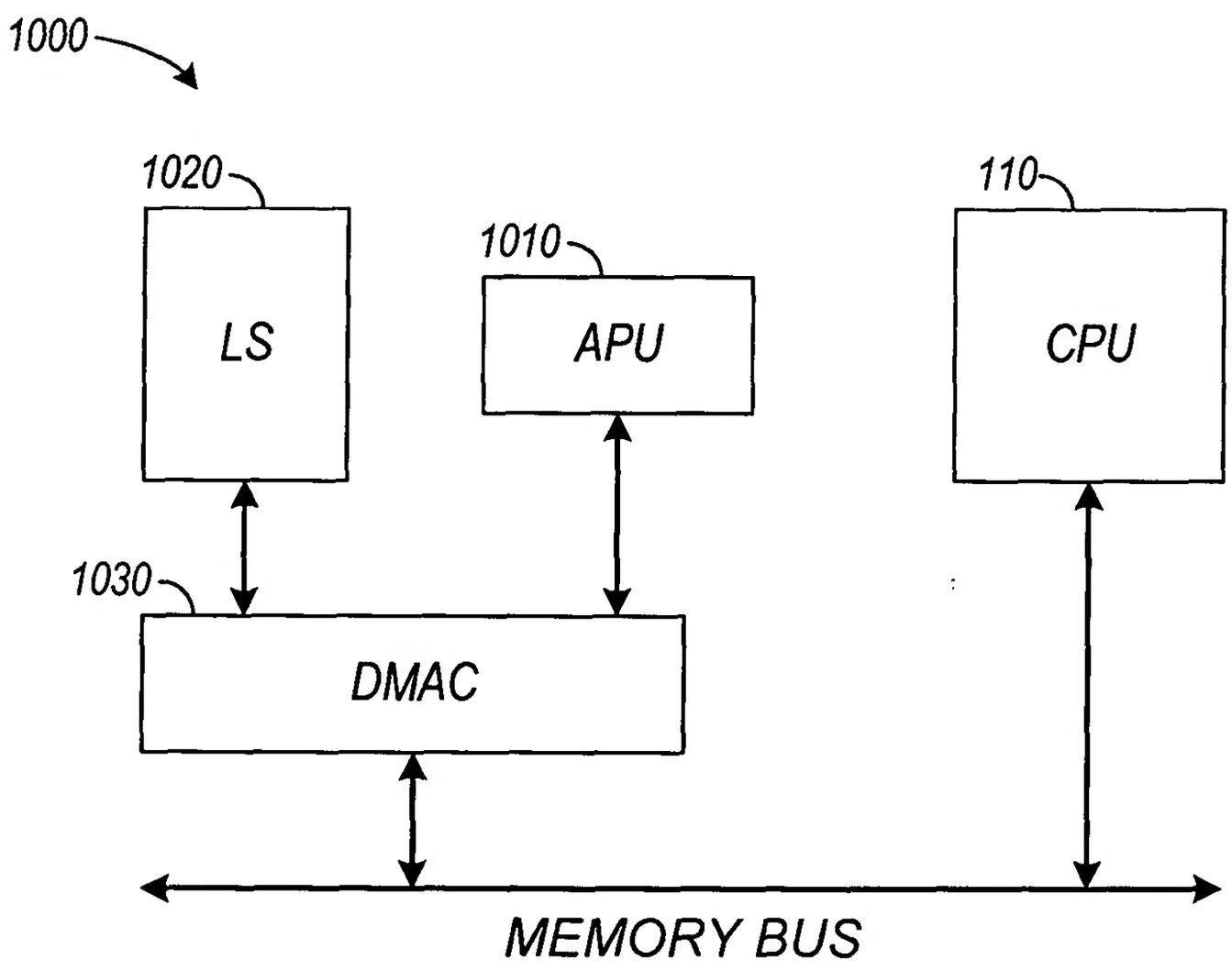
1000
1020
LS
1010
APU
110
CPU
1030
DMAC
MEMORY BUS

FIG. 1C

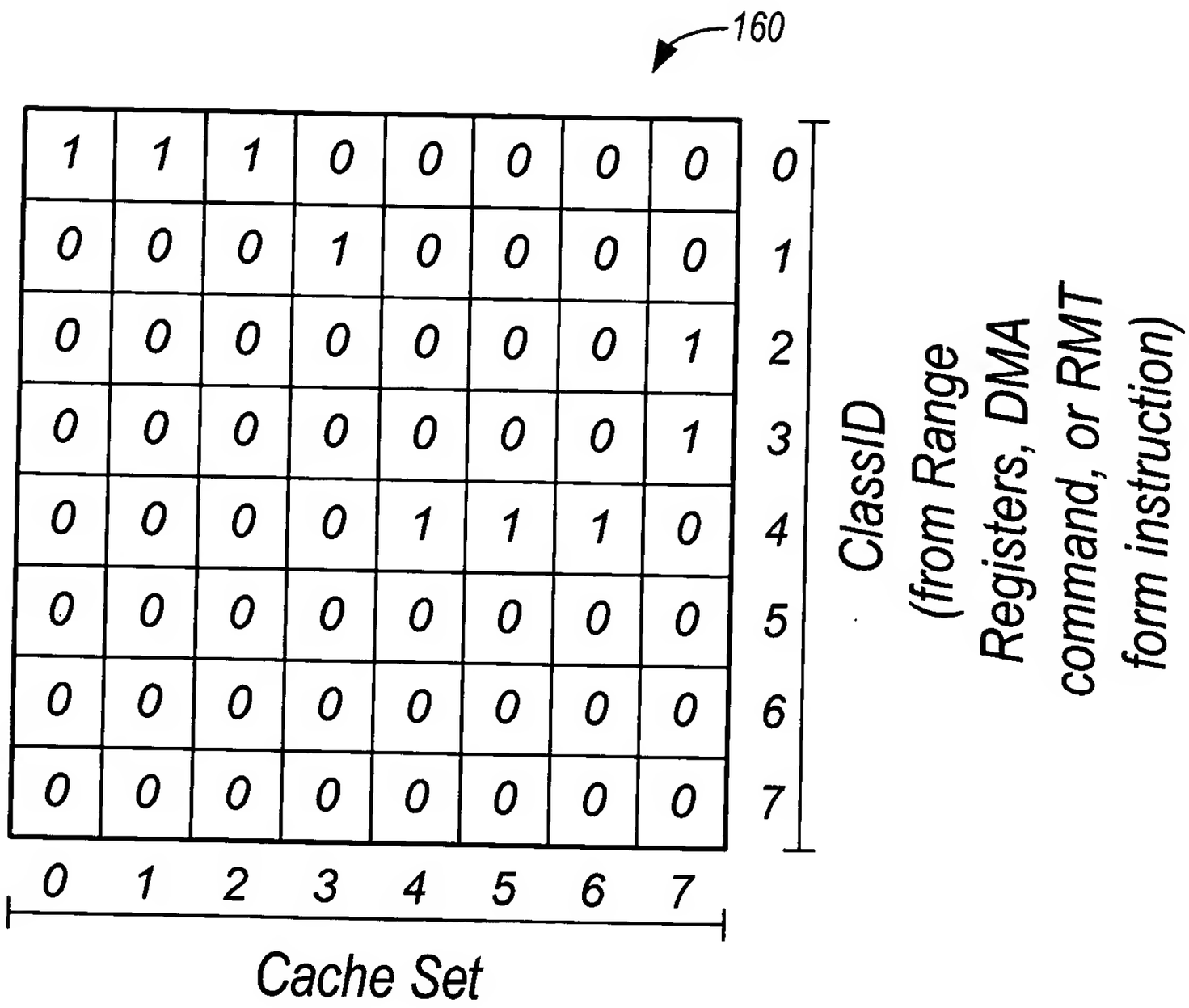

FIG. 2

Replacement Management Table: RMT_index	RMT_entry			
RMT_index 0	Set Enable Bits	v	b	a
RMT_index n	Set Enable Bits	v	b	a

FIG. 3

400

Range Start Register (RSR)

Range Start Register (high):																															
0								7	8																						31
Upper 32-bits of the starting address																															
Range Start Register (low):																															
32								39	40																						63
Lower 20-bits of the starting address																														*R*	*V*
																														0	0

FIG. 4

500

Range Mask Register

Range Mask Register:																															
0								7	8																						31
Lower 32-bits of the starting address																															
Range Mask Register:																															
32								39	40																						63
Lower 20-bits of the starting address																														0	0

FIG. 5A

ClassID Register (CIDR)

Class IDs:																															
0								7	8																						31
-	-																													*RclassID*	

FIG. 5B

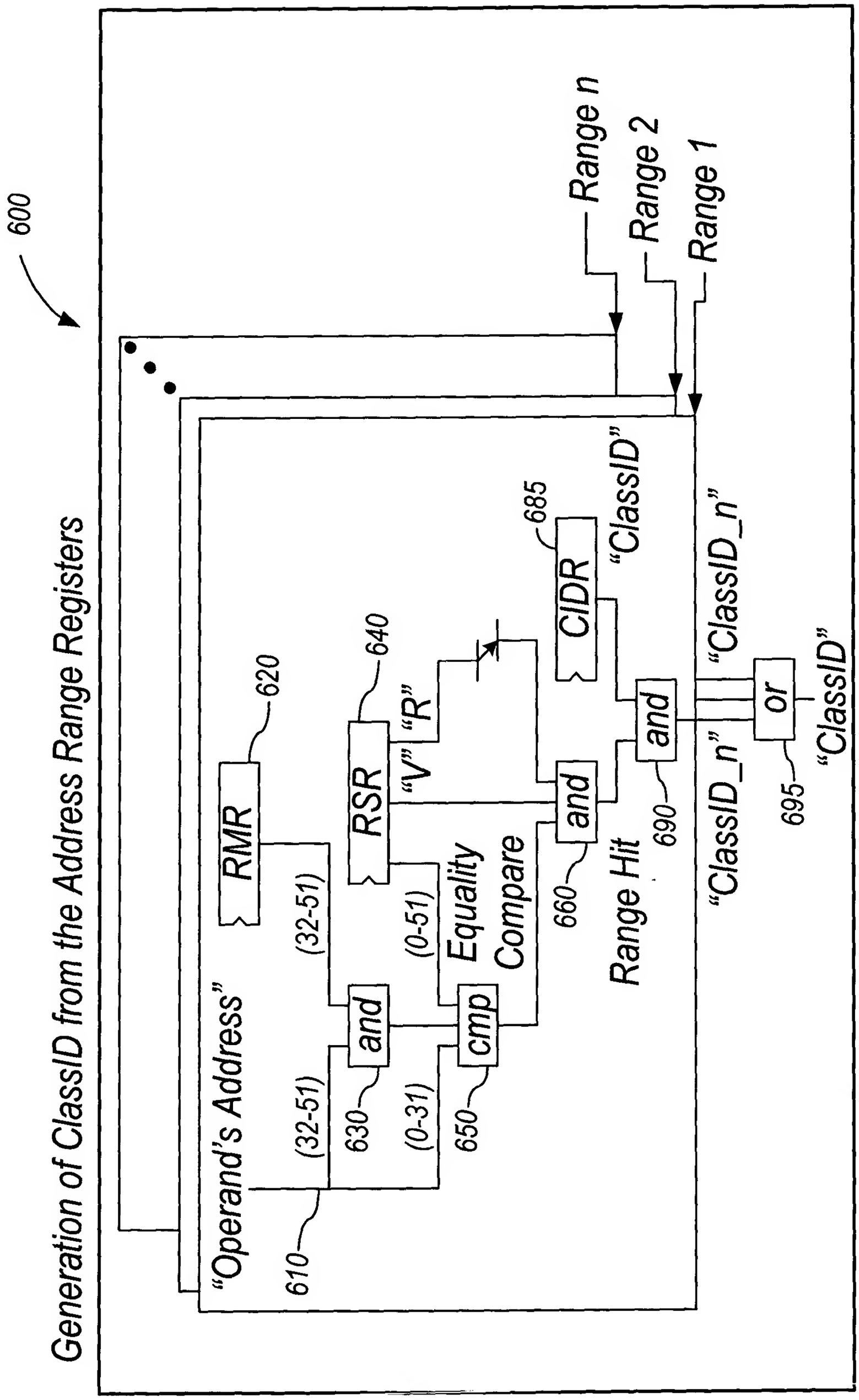
600
Generation of ClassID from the Address Range Registers
Range n
Range 2
Range 1
"Operand's Address"
(32-51)
610
RMR
620
RSR
640
"V"
"R"
(0-51)
(32-51)
630
and
(0-31)
650
cmp
Equality Compare
660
and
Range Hit
690
CIDR
685
"ClassID"
and
"ClassID_n"
"ClassID_n"
or
695
"ClassID"

FIG. 6

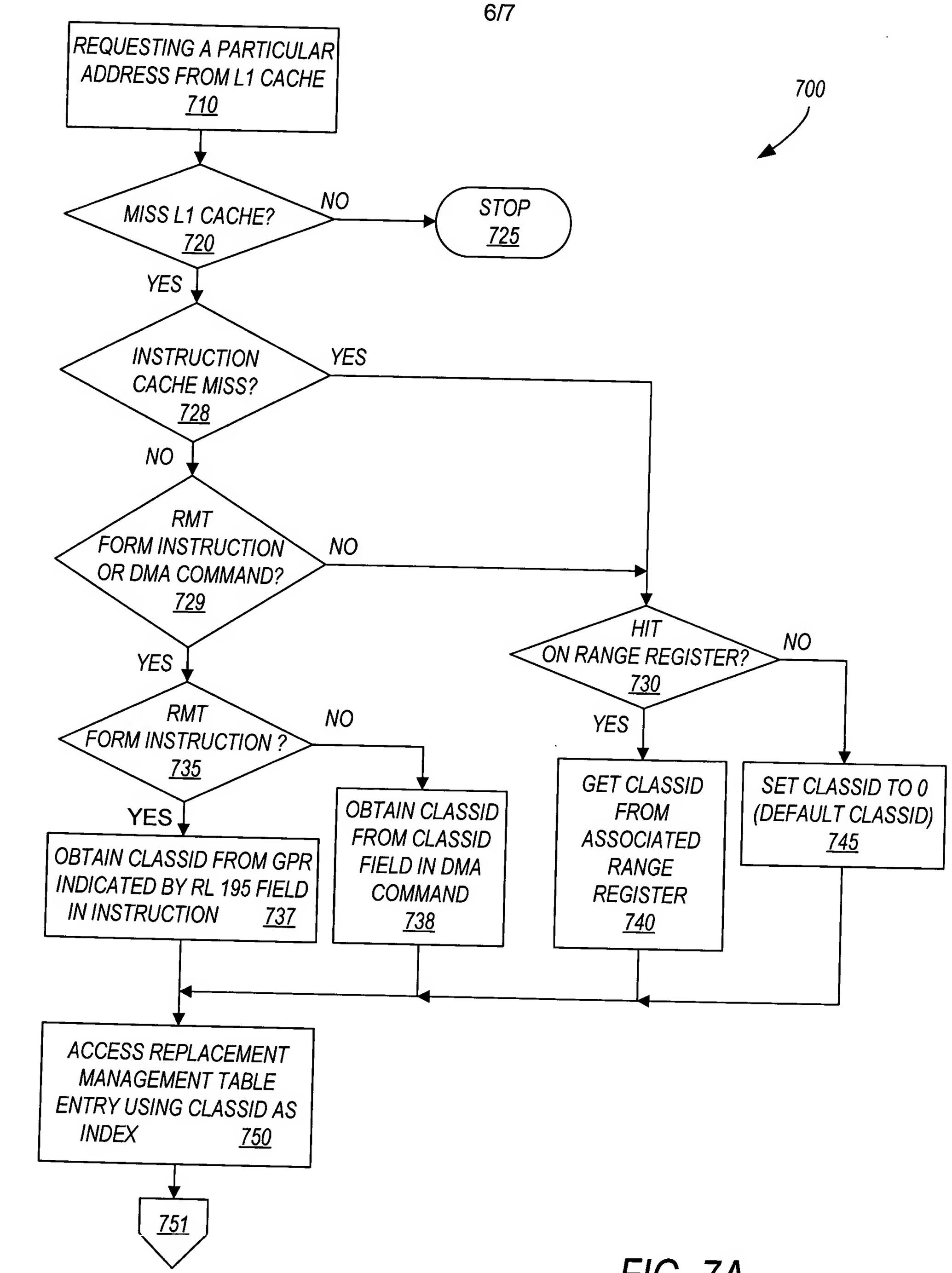
700
REQUESTING A PARTICULAR ADDRESS FROM L1 CACHE 710
MISS L1 CACHE? 720
NO
STOP 725
YES
INSTRUCTION CACHE MISS? 728
YES
NO
RMT FORM INSTRUCTION OR DMA COMMAND? 729
NO
YES
HIT ON RANGE REGISTER? 730
NO
YES
RMT FORM INSTRUCTION ? 735
NO
YES
OBTAIN CLASSID FROM GPR INDICATED BY RL 195 FIELD IN INSTRUCTION 737
OBTAIN CLASSID FROM CLASSID FIELD IN DMA COMMAND 738
GET CLASSID FROM ASSOCIATED RANGE REGISTER 740
SET CLASSID TO 0 (DEFAULT CLASSID) 745
ACCESS REPLACEMENT MANAGEMENT TABLE ENTRY USING CLASSID AS INDEX 750
751

FIG. 7A

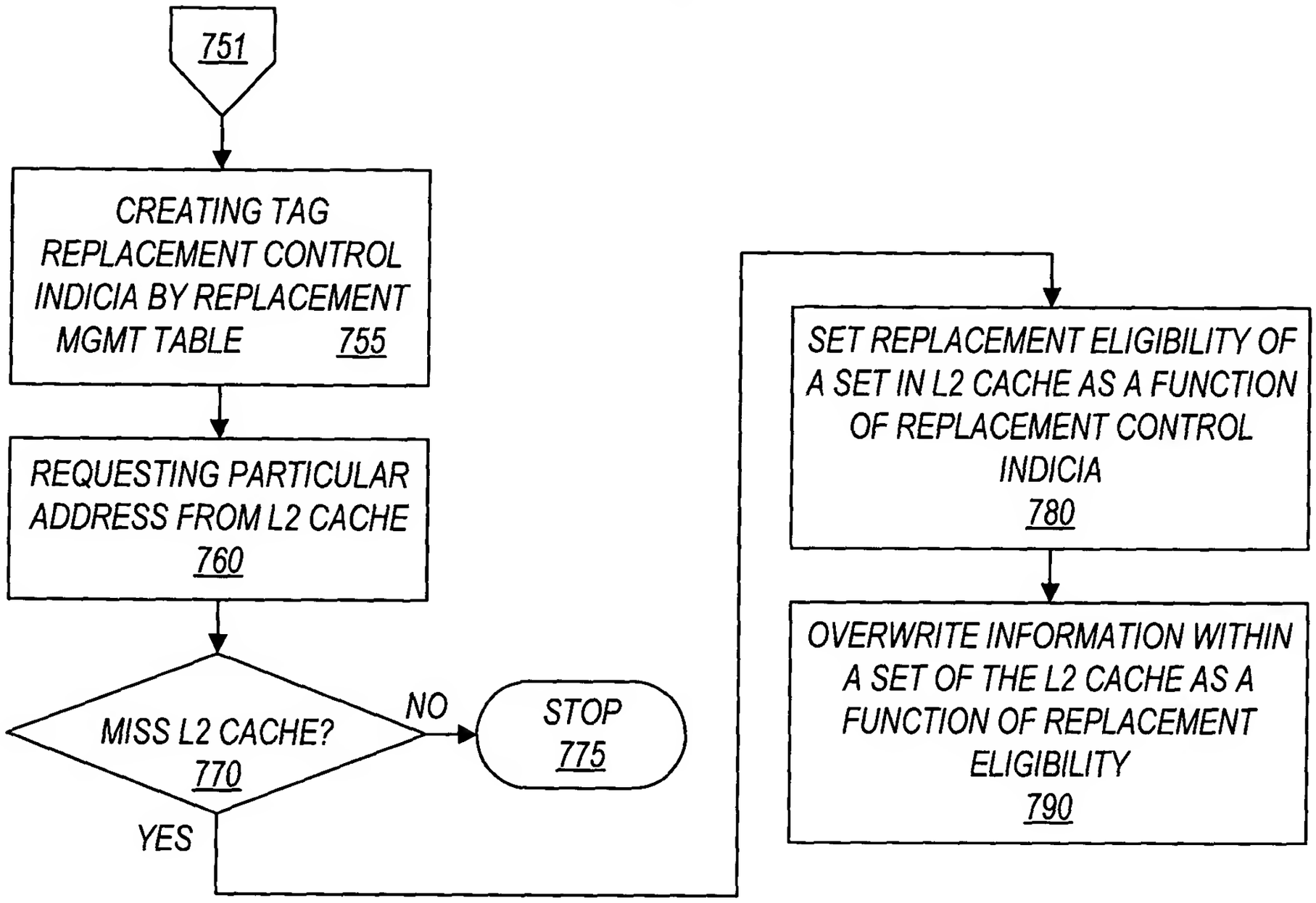
751
CREATING TAG REPLACEMENT CONTROL INDICIA BY REPLACEMENT MGMT TABLE 755
REQUESTING PARTICULAR ADDRESS FROM L2 CACHE 760
MISS L2 CACHE? 770
NO
STOP 775
YES
SET REPLACEMENT ELIGIBILITY OF A SET IN L2 CACHE AS A FUNCTION OF REPLACEMENT CONTROL INDICIA 780
OVERWRITE INFORMATION WITHIN A SET OF THE L2 CACHE AS A FUNCTION OF REPLACEMENT ELIGIBILITY 790

FIG. 7B